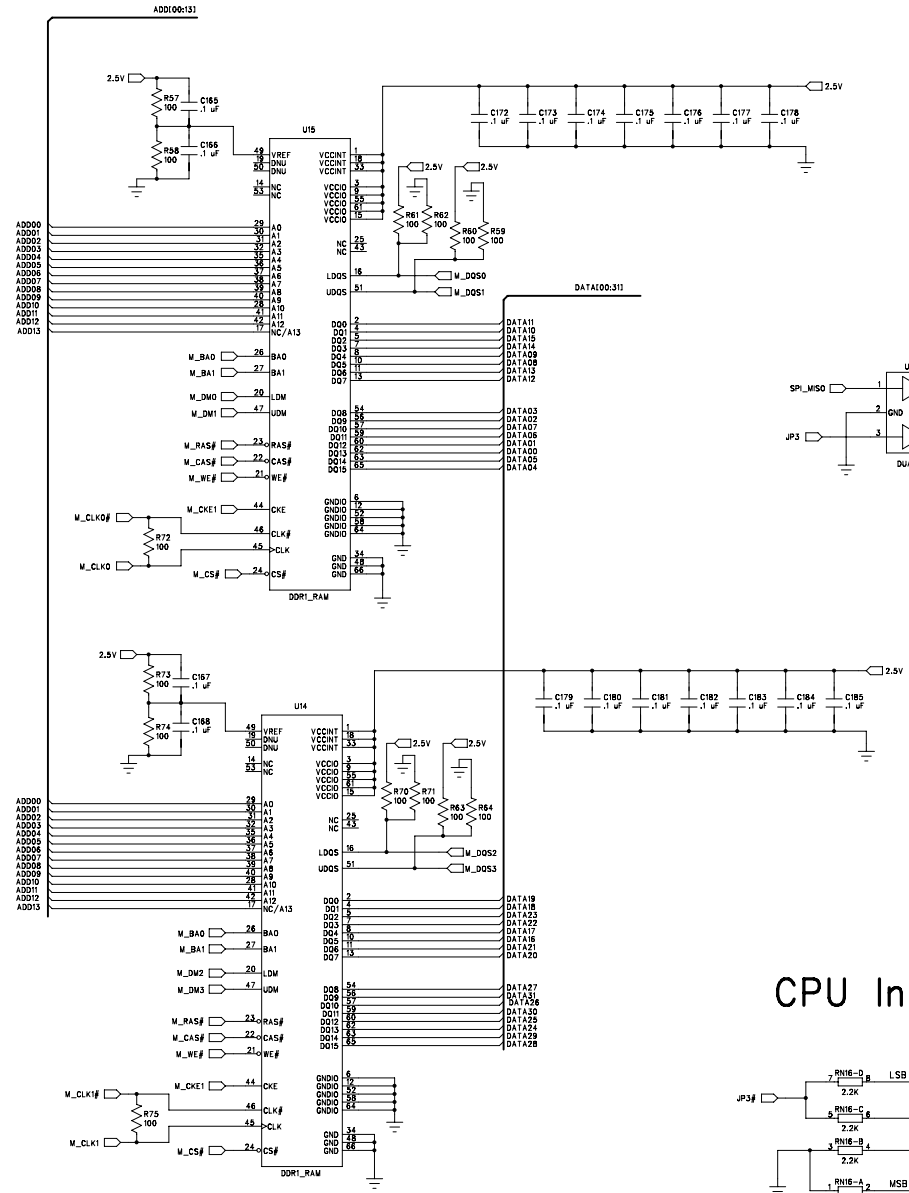
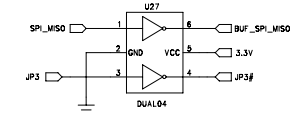
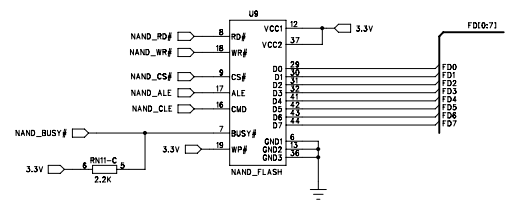




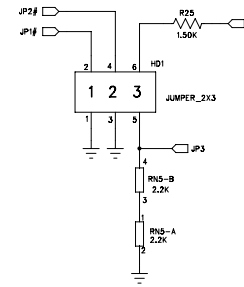
### DDR1 SDRAM



### NAND Flash

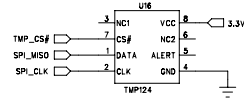


### Jumpers

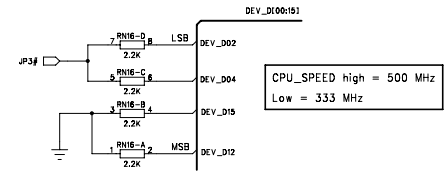


JP1 = Fast Boot to NAND Flash  
 JP2 = Enable console on COM1  
 JP3 = CPU Speed is 333 MHz

### Temp Sensor



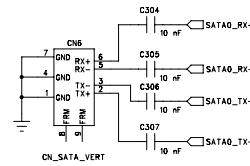
### CPU Initialization



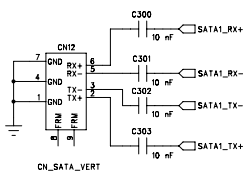
CPU\_SPEED high = 500 MHz  
 Low = 333 MHz

Technologic Systems	Date Aug. 6, 2007
Title: TS-7800	DDR RAM Flash
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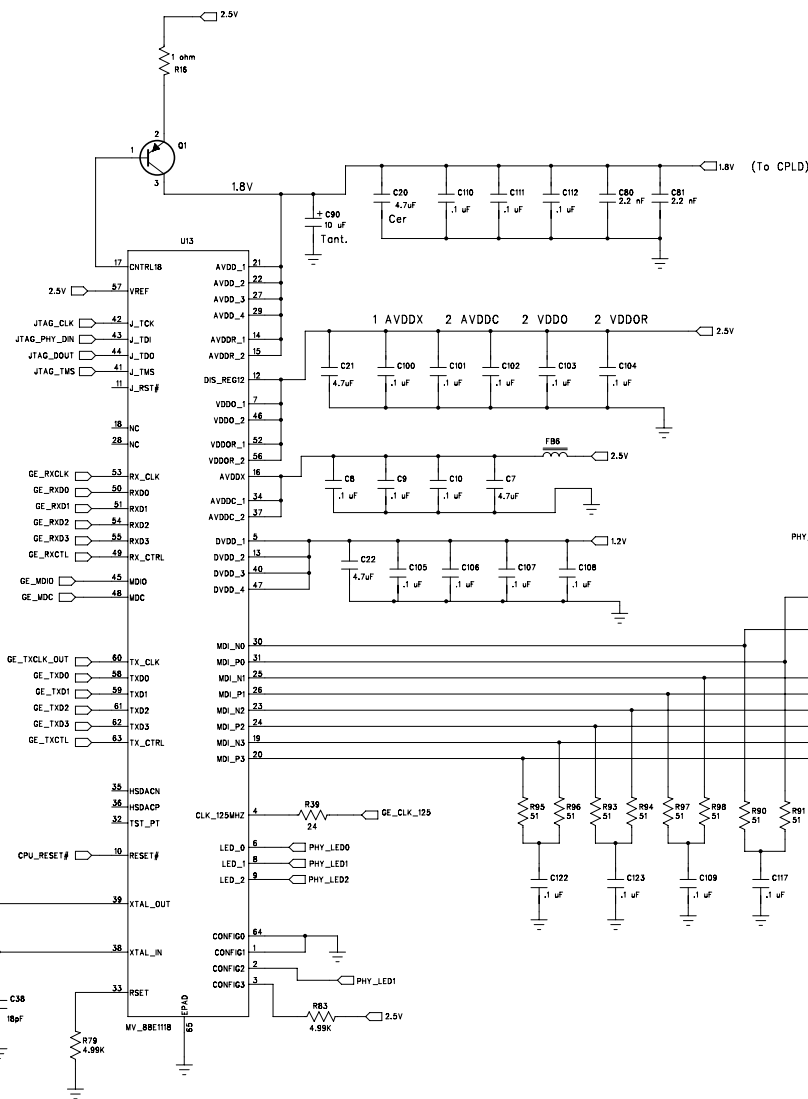
### SATA 0



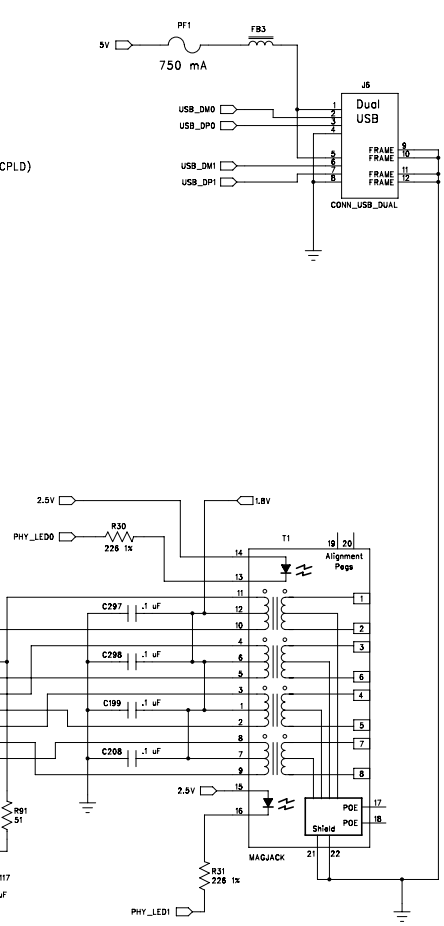
### SATA 1



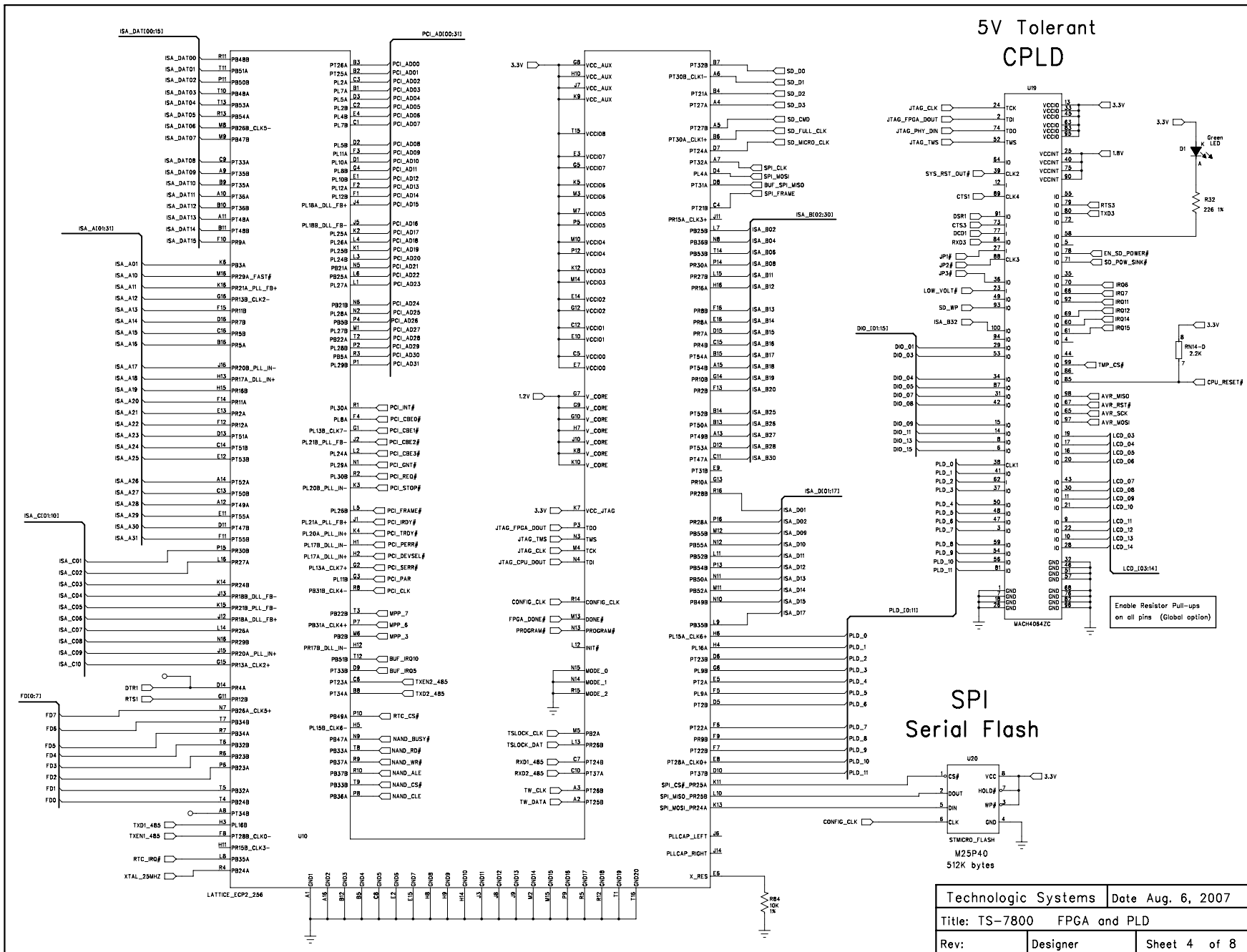
### 10/100/1000 Ethernet



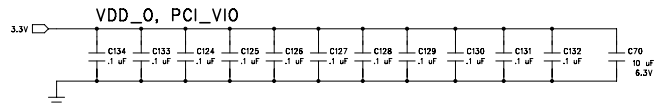
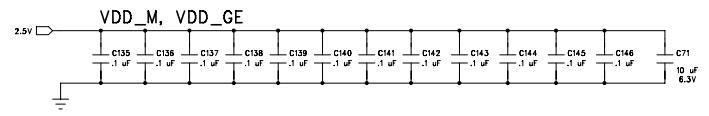
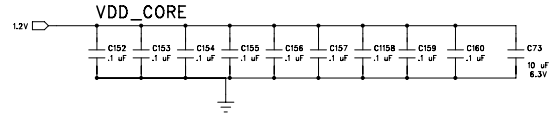
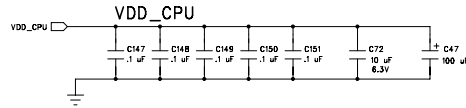
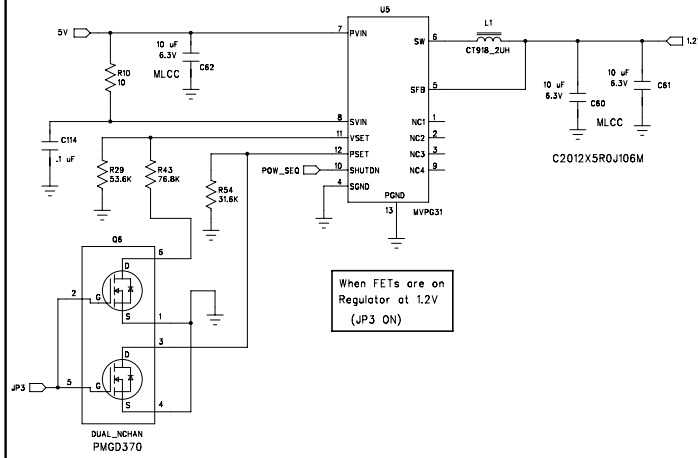
### USB Ports



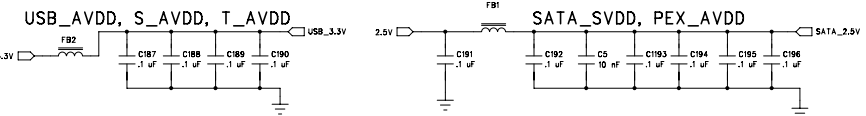
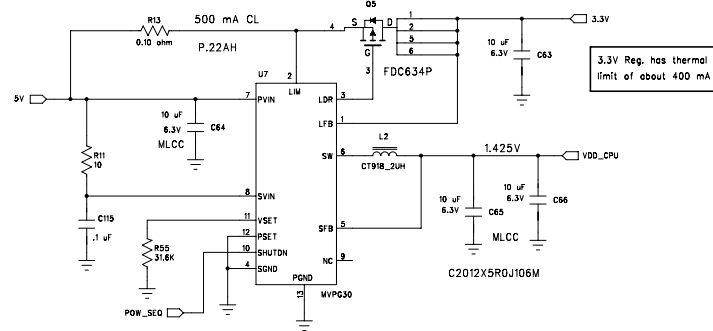
Technologic Systems	Date Aug. 6, 2007
Title: TS-7800 Ethernet, USB, SATA	
Rev:	Designer RLM Sheet 3 of 8



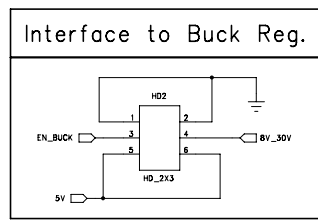
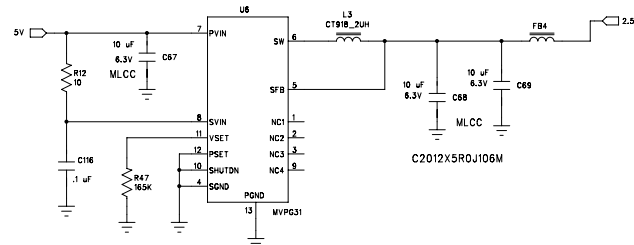
### 1.2V or 1.42V Power Supply



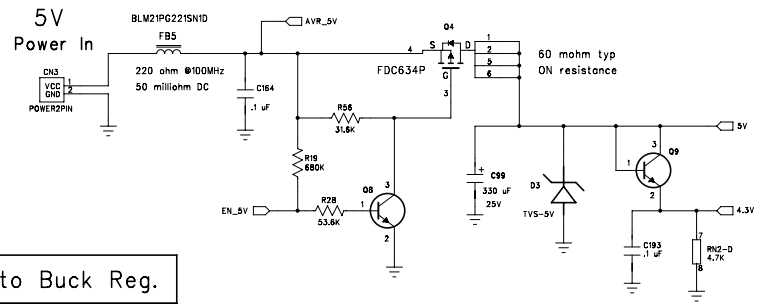
### 1.2V and 3.3V Power Supply



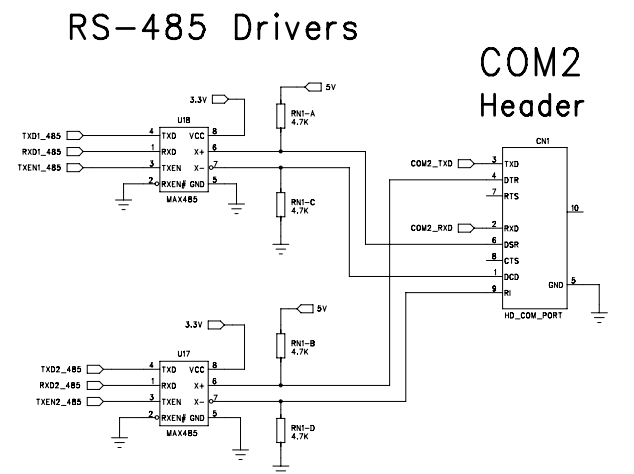
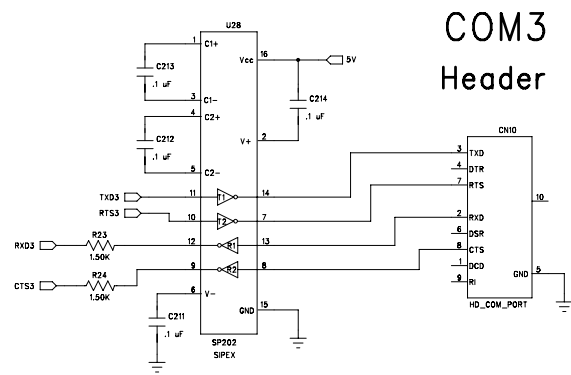
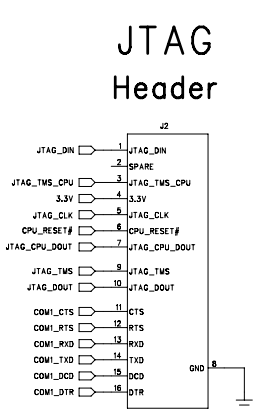
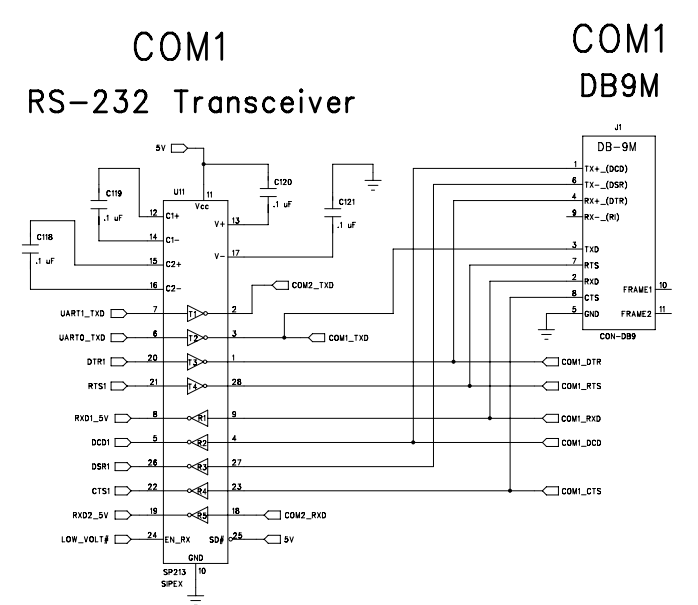
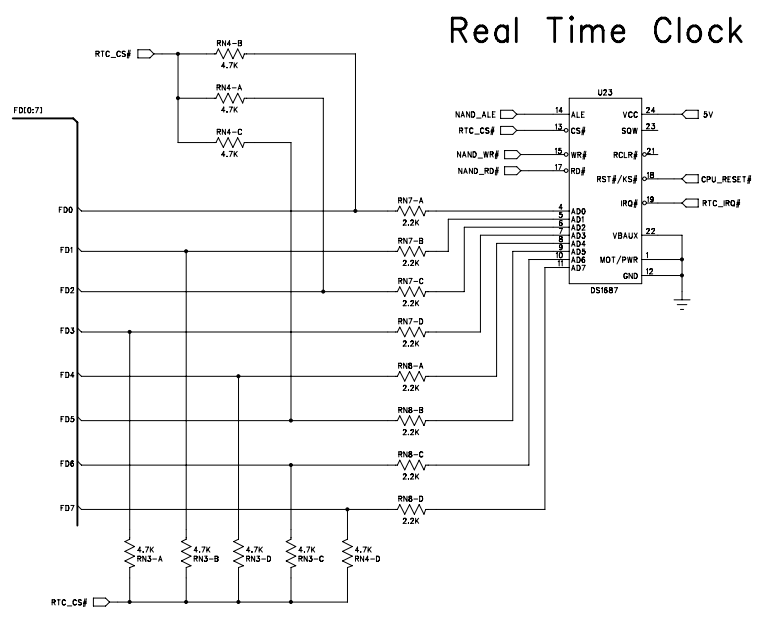
### 2.5V Power Supply



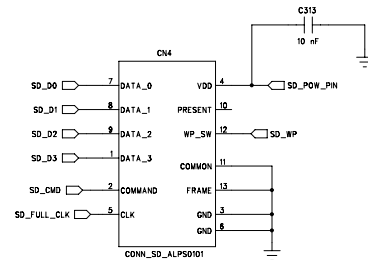
### 5V Switch



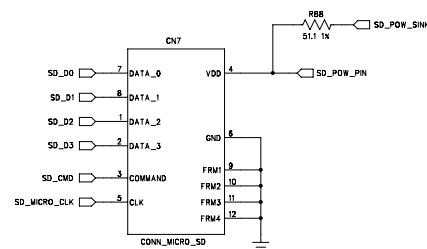
Technologic Systems		Date Aug. 6, 2007
Title: TS-7800 Power		
Rev:	Designer	Sheet 5 of 8



Technologic Systems	Date Aug. 6, 2007
Title: TS-7800 RTC, COM Ports, JTAG Header	
Rev:	Designer
	Sheet 6 of 8

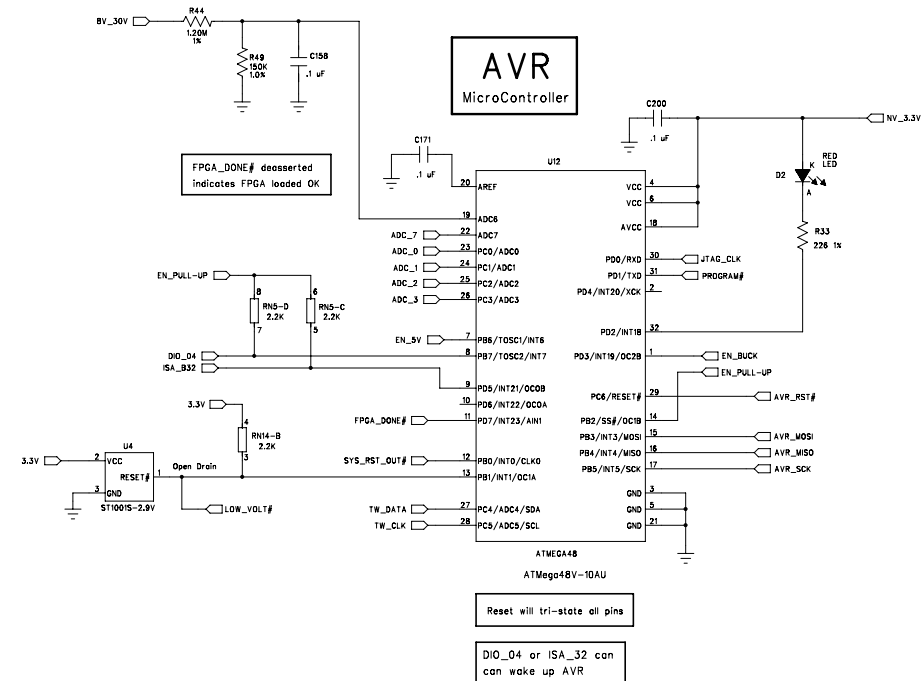
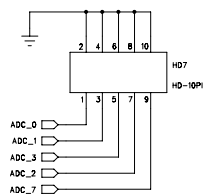


Full-Size SD Card Socket

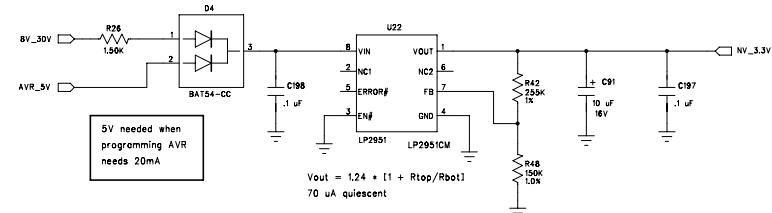


Micro SD Card Socket

5 Channel 12-bit A/D

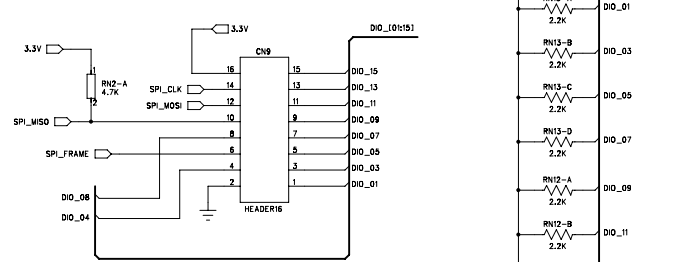


NV 3.3V Regulator for AVR



Technologic Systems	Date Aug. 6, 2007
Title: TS-7800 AVR, SD Card	
Rev:	Designer
	Sheet 7 of 8

### DIO Port



SPI\_MISO is 5V tolerant  
MOSI, CLK, and Frame  
are 3.3V level outputs

DIO\_01 thru DIO\_15 (odds) are always  
open drain outputs, initialized to high  
They can be used as inputs

DIO\_08 initializes to an input  
when output, active high-low  
It is programmable in or out

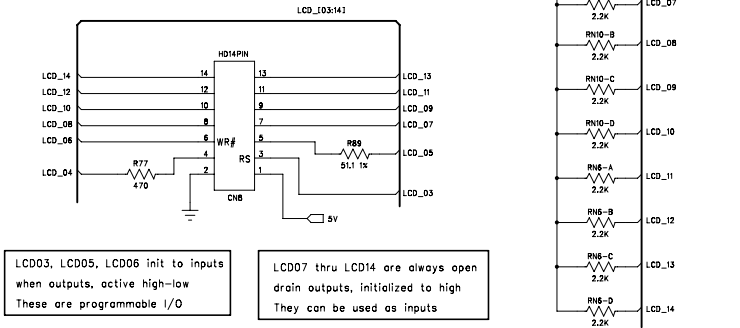
DIO\_04 is always input  
AVR drives pull-up on this pin

Pull-up resistors for  
the open drain outputs

Open drain outputs can  
sink 8 mA, but only source  
current thru resistor

All DIO lines are 5V tolerant

### LCD Port



LCD03, LCD05, LCD06 init to inputs  
when outputs, active high-low  
These are programmable I/O

LCD07 thru LCD14 are always open  
drain outputs, initialized to high  
They can be used as inputs

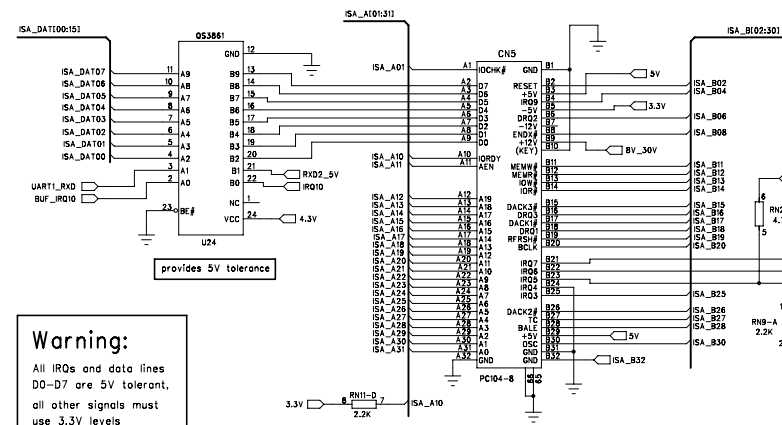
LCD04 is always output  
active high-low, init to zero

Pull-up resistors for  
the open drain outputs

Open drain outputs can  
sink 8 mA, but only source  
current thru resistor

All LCD lines are 5V tolerant

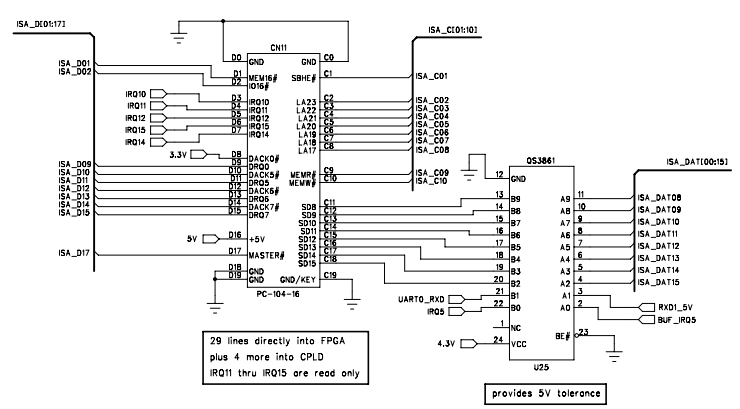
### PC/104 64-pin Connector



Warning:  
All IRQs and data lines  
D0-D7 are 5V tolerant,  
all other signals must  
use 3.3V levels  
IRQ3 must be 3.3V levels

51 lines directly into FPGA  
plus 3 more into CPLD (read only)  
(IRQ6, IRQ7 and ISA\_32)

### PC/104 40-pin Connector



29 lines directly into FPGA  
plus 4 more into CPLD  
IRQ11 thru IRQ15 are read only